WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

at least three independently accessible memory devices that can be independently tested, wherein at least one of the memory devices has a memory capacity differing from the other memory devices;

a plurality of signal lines for providing each of the memory devices with an address signal and a selection signal, for activating the memory devices; and

at least one inverter circuit each connected between a predetermined one of the memory devices and a predetermined one of the signal lines for providing the selection signal, wherein the inverter circuit inverts the selection signal.

2. The semiconductor device according to claim 1, wherein the predetermined memory device is the memory device excluding the one having a test period that is longest among the at least three memory devices.